REMARKS

By way of overview, claims 1-22 have been examined, with claims 1-3 and 5-22 rejected and claim 4 objected to. Claims 11-14 and 21 are canceled, and thus claims 1-10, 15-20, and 22 are now pending.

Claims 6-10, 12, and 21 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Also, the specification is objected to because in the paragraph bridging pages 4 and 5, a serial number and filing date are lacking. It is believed that the amendments to the claims and specification overcome this rejection and objection.

Turning to the prior art rejection, claims 1-3, 5-8, and 10-22 are rejected under 35 U.S.C. § 102(b) as being anticipated by Rueth et al. (U.S. Patent No. 5,228,054). While not conceding this validity of the rejection, and merely to advance prosecution, applicant has canceled claims 11-14 and 21. With regard to claims 1-3, 5-8, 10, 15-20, and 22, applicant respectfully traverses this rejection for the reasons set forth below.

Claim 6:

Claim 6 recites, in general, a pseudo-random sequence generator having a linear feedback shift register (LFSR) that generates a first pseudo-random sequence and a sequence of vectors, a first mask circuit that generates a second pseudo-random sequence by selectively combining vector values of each vector of the sequence of vectors, a second mask circuit that generates a third pseudo-random sequence by selectively combining vector values of each vector of the sequence of vectors, and logic circuits that generate a fourth pseudo-random sequence from the second pseudo-random sequence and the third pseudo-random sequence.

Rueth does not disclose, or even suggest, the claimed second mask circuit. As shown in Fig. 1 of the present application, the claimed first mask circuit 130a and second mask circuit 130b each receive the sequence of vectors from the LFSR 120. While Rueth does teach a single mask

circuit 30 in Fig. 2 (or 30' in Fig. 5) that receives a sequence of vectors from the LSSR 10, there is no second mask circuit. Thus, claim 6 is patentable over Rueth.

Claim 18:

Claim 18 recites, in general, a pseudo-random sequence generator having a LFSR that generates a pseudo-random output sequence and a sequence of vectors, a first logic that combines vector values of each vector of the sequence of vectors in a first way to produce a first sequence, a second logic that combines the vector values of each vector of the sequence of vectors in a second way to produce a second sequence, and a third logic that selectively combines the first sequence and the second sequence to produce a third sequence that differs from the pseudorandom output sequence.

Rueth does not disclose, or even suggest, the claimed second logic. As shown in Fig. 1 of the present application, the claimed first logic 130a and second logic 130b each receive the sequence of vectors from the LFSR 120. While Rueth does teach a single logic 30 in Fig. 2 (or 30' in Fig. 5) that receives a sequence of vectors from the LSSR 10, there is no second logic that combines the vector values of each vector of the sequence of vectors received from the LSSR 10 in a second way to produce a second sequence. Other than mask circuit 30, comparator 20 is the only circuit element that receives the sequence of vectors from the LSSR 10, and comparator 20 does not combine the vector values to produce a sequence. Thus, claim 18 is patentable over Rueth.

Claims 15 and 1:

Claim 15 recites, in general, a method of operating a LFSR including generating a sequence of vectors, each vector constituting the output of at least some of the stages of the LFSR, selectively combining vector values of each vector of the sequence of vectors in a first way to produce a first sequence, selectively combining the vector values of each vector of the sequence of vectors in a second way to produce a second sequence, and selectively combining the first sequence and the second sequence to produce a third sequence that differs from the pseudo-random output sequence.

Similarly, claim 1 recites, in general, in a pseudo-random sequence generator having a LFSR that generates a first pseudo-random sequence, including selectively combining vector values of each vector of a sequence of vectors in a first way to produce a second pseudo-random sequence, selectively combining vector values of each vector of the sequence of vectors in a second way to produce a third pseudo-random sequence, and selectively outputting bits of the second pseudo-random sequence and at least one bit of the third pseudo-random sequence to form a fourth pseudo-random sequence, wherein the fourth pseudo-random sequence differs from the first pseudo-random sequence.

Rueth does not disclose, or even suggest, selectively combining the vector values of each vector of the sequence of vectors in a second way to produce a second sequence (third sequence in claim 1). Again, as shown in Fig. 1 of the present application, vector values of each vector of the sequence of vectors are selectively combined by the mask circuit 130a in a first way to produce a first sequence (second sequence in claim 1), and are selectively combined by the mask circuit 130b in a second way to produce a second sequence (third sequence in claim 1). While Rueth does teach selectively combining vector values of each vector of the sequence of vectors by the mask circuit 30 (see Fig. 2) in a first way to produce a first (second in claim 1) sequence, it does not teach, or even suggest, selectively combining vector values of each vector of the sequence of vectors in a second way to produce a second (third in claim 1) sequence, as required by claims 15 and 1. Thus, claims 15 and 1 are patentable over Rueth.

Dependent Claims:

Each of claims 2, 3, 5, 7, 8, 10, 16, 17, 19, 20, and 22 depend from one of independent claims 1, 6, 15, and 18, and thus is patentable for the same reasons as the claim from which it depends.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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